TPD4S012 4-Channel ESD Solution for USB-HS/USB OTG/USB Charger Interface

1 Features

- Integrated ESD Clamps on all Pins
- USB Signal Pins (D+, D–, ID)
  - 0.8-pF Line Capacitance
- Supports Data Rates in Excess of 480 Mbps
- IEC 61000-4-2 ESD Protection (Level 4 Contact)
  - ±10-kV IEC 61000-4-2 Contact Discharge
- IEC 61000-4-5 Surge
  - 3 Amps Peak Pulse Current

2 Applications

- Cellular Phones
- Digital Cameras
- Global Positioning Systems (GPS)
- Portable Digital Assistants (PDA)
- Portable Computers

3 Description

The TPD4S012 is a four-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array for USB chargers and USB On-The-Go (OTG) interfaces.

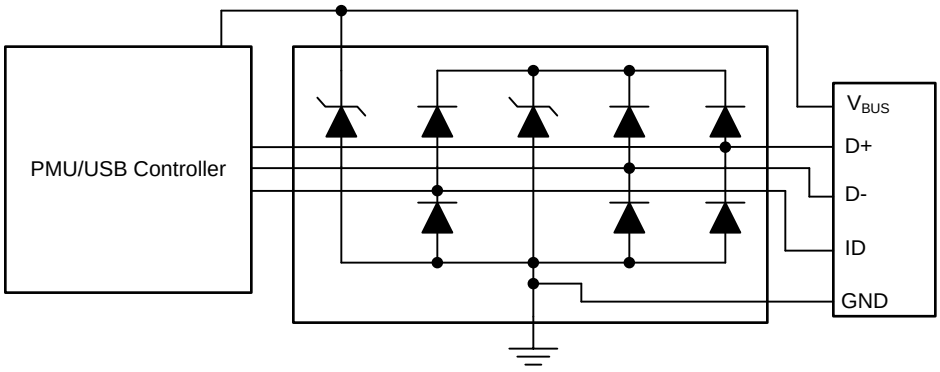
The TPD4S012 provides IEC 61000-4-2 system level ESD Protection featuring 15 V tolerance on the V_{BUS} line. The device is ideal for providing circuit protection for USB charger and OTG applications due to its high-voltage tolerance at the V_{BUS} line and small flow-through package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4S012	SON (6)	1.45 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

Changes from Revision A (November 2009) to Revision B **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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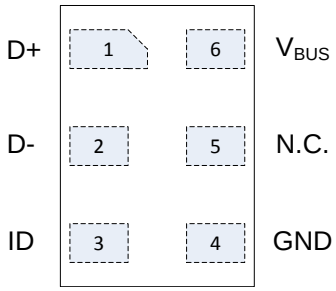
5 Pin Configurations and Functions

DRY PACKAGE
(TOP VIEW)



N.C. – Not internally connected

D+, D–, and ID pins are exact equivalent ESD clamp circuits. Any of these pins can be connected to any other D+, D–, or ID pin if it becomes easier to route the traces from the USB connector.

Pin Functions

PIN		TYPE	DESCRIPTION
DRY PIN NO.	NAME		
1	D+	ESD clamp	Provides ESD protection to the high-speed differential data lines
2	D–	ESD clamp	Provides ESD protection to the high-speed differential data lines
3	ID	ESD clamp	Provides ESD protection to the high-speed differential data lines
4	GND	PWR	Ground
5	N.C.	–	Not internally connected
6	V_{BUS}	ESD clamp	ESD clamp for high-voltage tolerant V_{BUS} line(s)

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
	V_{BUS} voltage tolerance	V_{BUS} pin	–0.3	20	V
	IO voltage tolerance	D+, D–, ID pins	–0.3	6	V
T_A	Operating free-air temperature range		–40	85	°C
	IEC 61000-4-2 Contact Discharge	D+, D–, ID		±10	kV
		V_{BUS} pin		±10	kV
	IEC 61000-4-2 Air-Gap Discharge	D+, D–, ID		±10	kV
		V_{BUS} pin		±9	kV
	IEC 61000-4-5 Surge (t_p = 8/20 µs)	Peak pulse Power (All pins)		60	W
		Peak pulse current (All Pins)		3	A

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2.5	2.5	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
T_A Operating free-air Temperature Range		–40	85	°C
Operating Voltage	V_{BUS} Pin	0	15	V
	D+, D–, ID Pins	0	5.5	

6.4 Thermal Information

THERMAL METRIC(1)		TPD4S012 DRY 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	461.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	219.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	343.7	
ψ_{JT}	Junction-to-top characterization parameter	162.5	
ψ_{JB}	Junction-to-board characterization parameter	343.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VBUS}	V_{BUS} operating current	V_{BUS} = 19 V	D+, D–, ID pins open		0.1	0.5	µA
I_{IO}	IO port current	V_{IO} = 2.5 V, V_{BUS} = 5 V	D+, D–, ID pins		0.1	0.5	µA
V_D	Diode forward voltage	I_{IO} = 8 mA	D+, D–, ID pins (lower clamp diode)	0.6	0.8	0.95	V
C_{VBUS}	V_{BUS} pin capacitance	V_{BUS} = 5 V			11	15	pF
C_{IO}	IO capacitance	V_{IO} = 2.5 V	D+, D–, ID pins		0.8	1	pF
R_{DYN}	Dynamic resistance	I_{IO} = 1.5 A	D+, D–, ID, and V_{BUS} pins, including central clamp dioded during positive ESD pulse		1.2		Ω
		I_{IO} = 1 A	D+, D–, ID, and V_{BUS} pins, including central clamp diode during negative ESD pulse		1		
V_{BR}	Breakdown voltage	I_{IO} = 1 mA	D+, D–, ID pins	6	9		V
			V_{BUS} pin(s)	20	24		

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6.6 Typical Characteristics

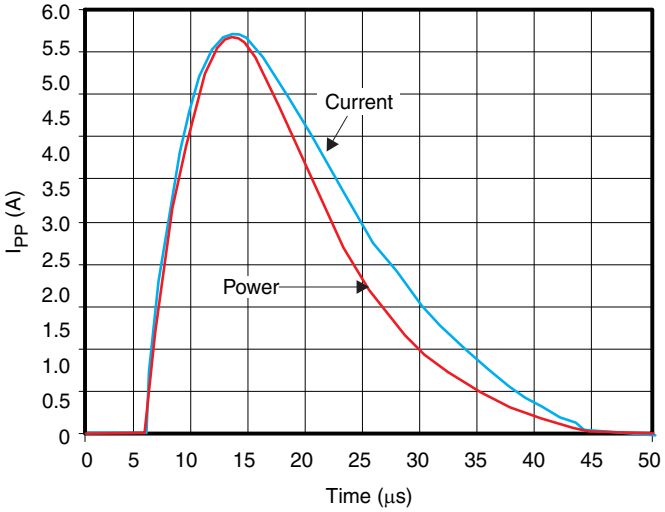

Figure 1. Peak Pulse Power Waveform at the D+, D–, or ID Pin

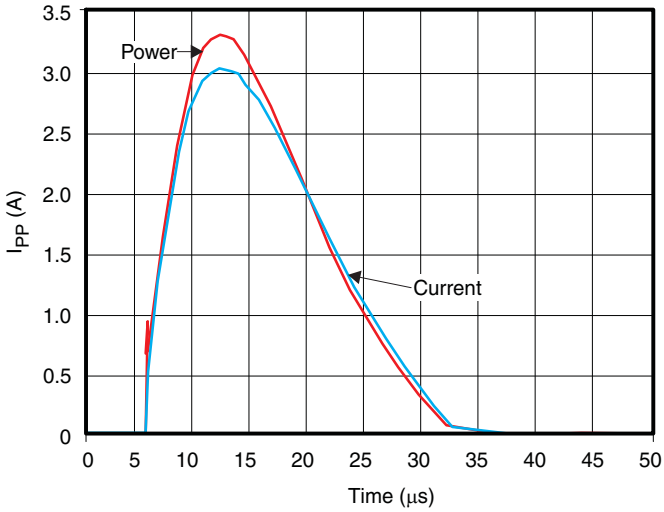

Figure 2. Peak Pulse Power Waveform at the V_{BUS} Pin

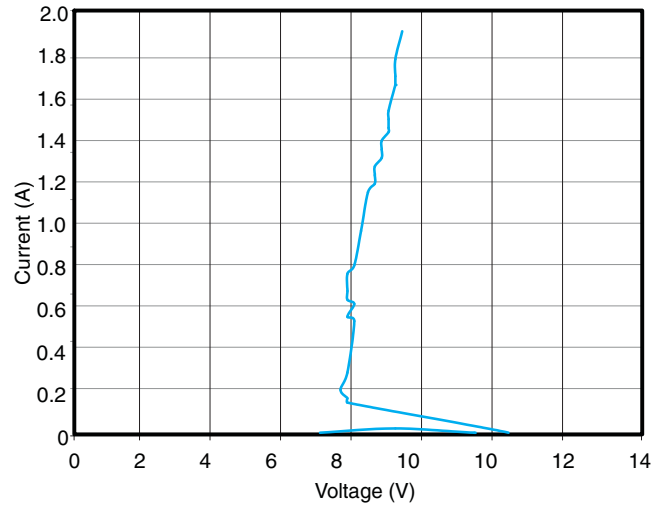

Figure 3. D+, D–, or ID Clamp Voltage Under ESD Event

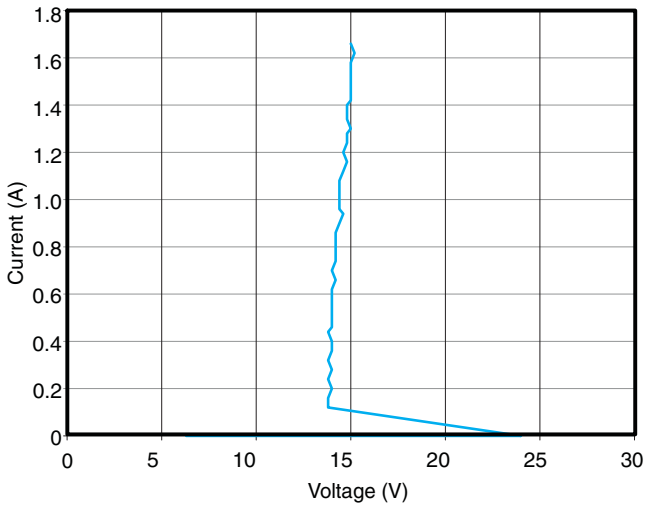

Figure 4. V_{BUS} Clamp Voltage Under ESD Event

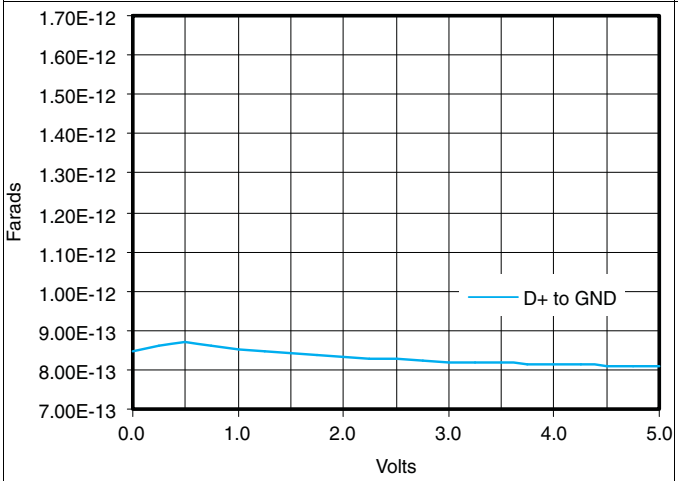

Figure 5. D+, D–, or ID Capacitance, T_A = 27°C

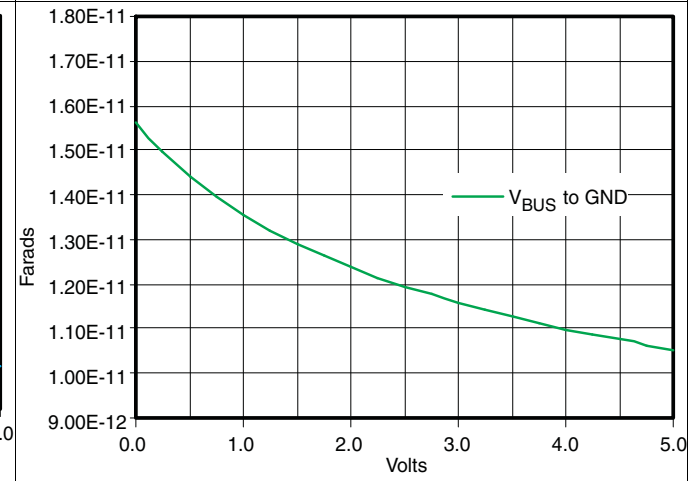

Figure 6. V_{BUS} Capacitance, T_A = 27°C

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Typical Characteristics (continued)

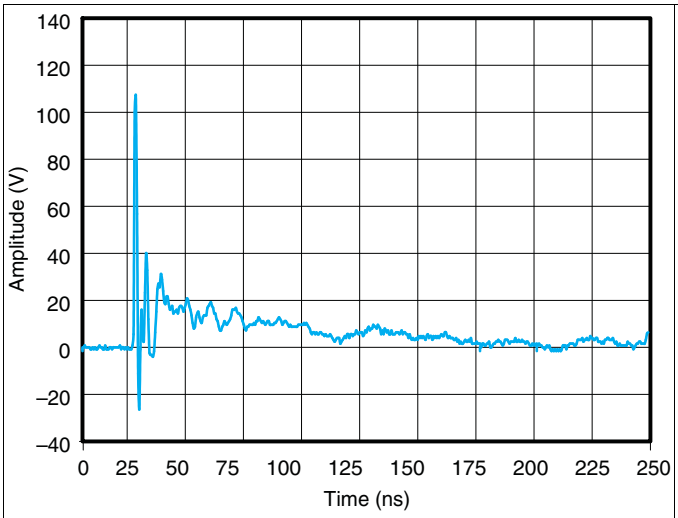


Figure 7. IEC Clamping Waveform, 8 kV Contact, D+, 25 ns/div

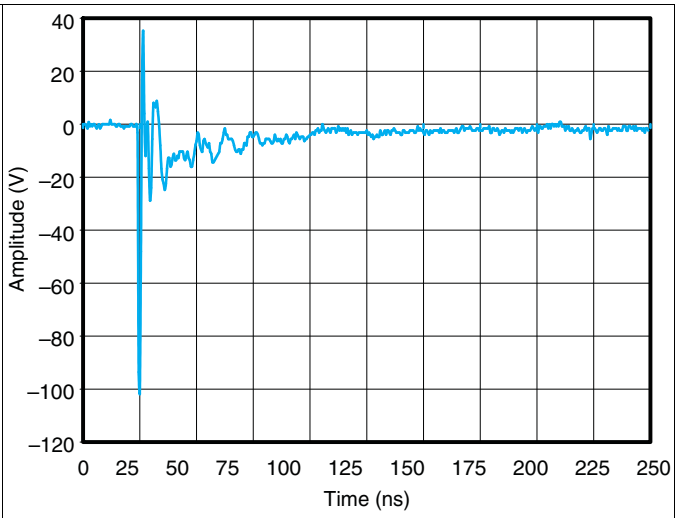


Figure 8. IEC Clamping Waveform, –8 kV Contact, D+, 25 ns/div

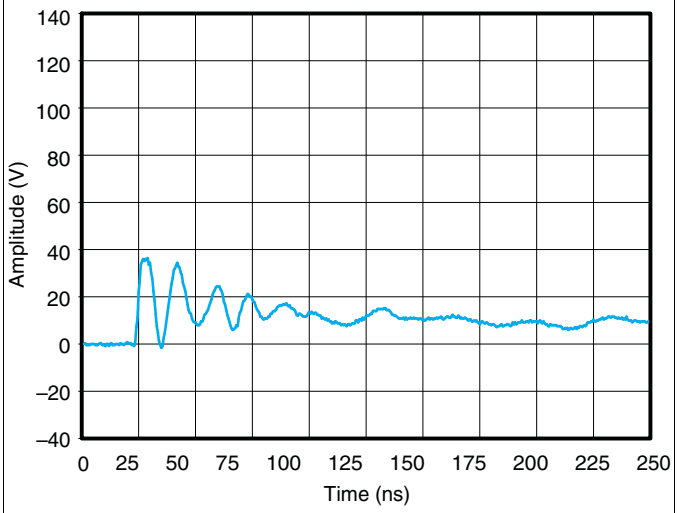


Figure 9. V_{BUS} IEC Clamping Waveform, 8 kV Contact, 25 ns/div

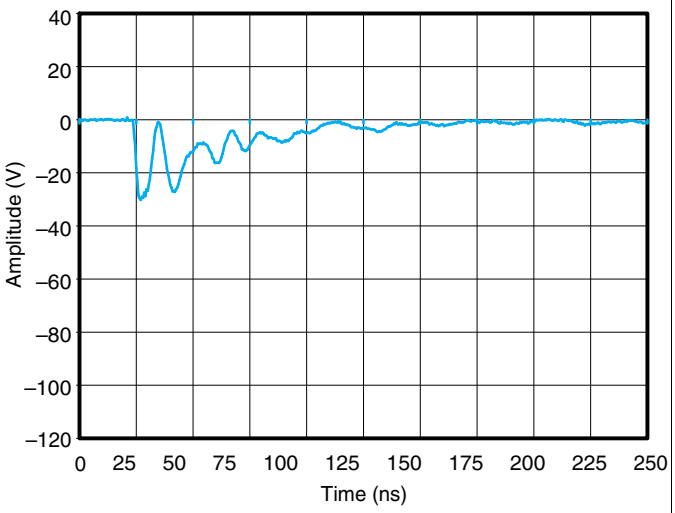


Figure 10. V_{BUS} IEC Clamping Waveform, –8 kV Contact, 25 ns/div

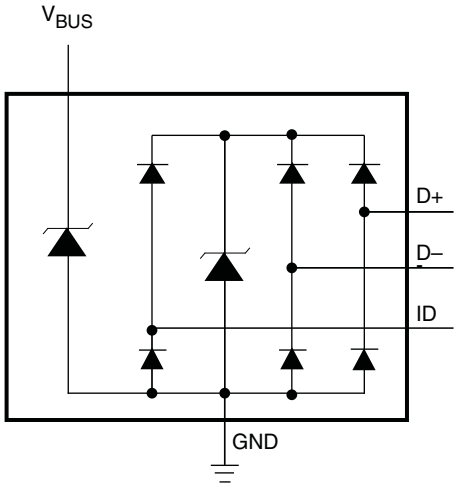
7 Detailed Description

7.1 Overview

The TPD4S012 is a four-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array for USB chargers and USB On-The-Go (OTG) interfaces.

The TPD4S012 provides IEC 61000-4-2 system level ESD Protection featuring 15 V tolerance on the V_{BUS} line. The device is ideal for providing circuit protection for USB charger and OTG applications due to its high-voltage tolerance at the V_{BUS} line and small flow-through package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated ESD Clamps

Integrated ESD Clamps on the D+, D–, V_{BUS}, and ID pins provide single-chip ESD protection for USB High Speed, USB-OTG, and USB charger interfaces.

7.3.2 USB Signal Pins

D+, D– and ID USB Signal pins have low capacitance (0.8 pF Typ).

7.3.3 V_{BUS} Line

The V_{BUS} line has a 11 pF (Typ) capacitance.

7.3.4 Supports Data Rates in Excess of 480 Mbps

The low capacitance (0.8 pF Typ) of the data lines supports speeds in excess of 480 Mbps.

7.3.5 IEC 61000-4-2 (Level 4 Contact)

IEC 61000-4-2 (Level 4 contact) system level ESD compliance measured at the D+, D– and ID pins is rated for ±10 kV contact and air-gap discharge.

7.3.6 IEC 61000-4-5 Surge

IEC 61000-4-5 system level surge compliance measured at D+, D–, ID, and V_{BUS} pins rated to 3 A of peak pulse current.

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7.4 Device Functional Modes

The TPD4S012 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diode's V_f. During ESD events, voltages as high as ±10 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4S012 (usually within 10's of nano-seconds), the device reverts to passive.

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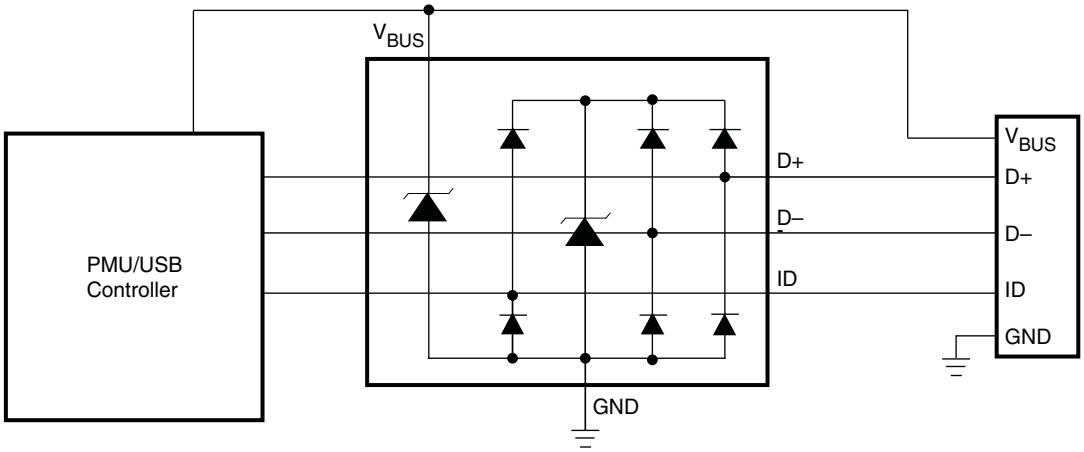
8 Applications and Implementation

8.1 Application Information

The TPD4S012 is a four-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array for USB chargers and USB On-The-Go (OTG) interfaces.

The TPD4S012 provides IEC 61000-4-2 system level ESD Protection featuring 15 V tolerance on the V_{BUS} line. The device is ideal for providing circuit protection for USB charger and OTG applications due to its high-voltage tolerance at the V_{BUS} line and small flow-through package.

8.2 Typical Application



If the ID pin is not used, it can be left floating.

Figure 11. Typical Application Schematic

8.2.1 Design Requirements

For this design example, a single TPD4S012 is used to protect all pins of a micro/mini USB connector.

Given the USB application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on D+, D–, and ID	0 V to 5 V
Signal range on V_{BUS}	0 V to 5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range on D+, D-, ID and V_{BUS} pins

The TPD4S012 has 3 pins which support 0 to 5.5 V signals, these are suited for the D+, D–, and ID pins. The V_{BUS} pin is suitable for the VBUS line, and has the benefit of being tolerant of voltages up to 16 V

8.2.2.2 Operating Frequency

The 0.8 pF (Typ) of the TPD4S012 support data rates in excess of 480 Mbps.

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8.2.3 Application Curve

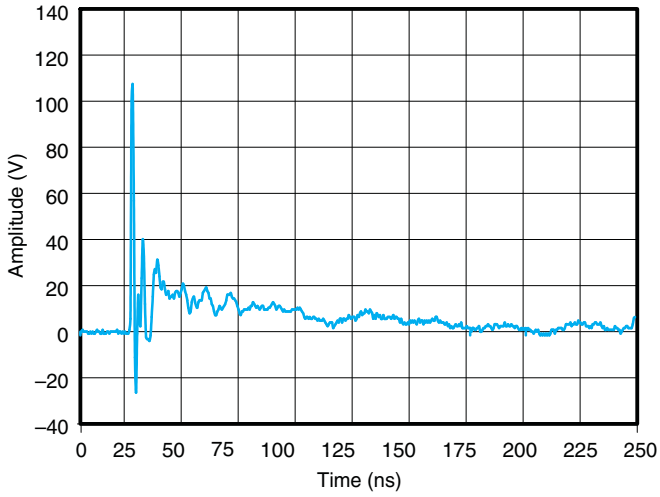

Figure 12. IEC Clamping Waveform, 8 kV Contact, D+, 25 ns/div

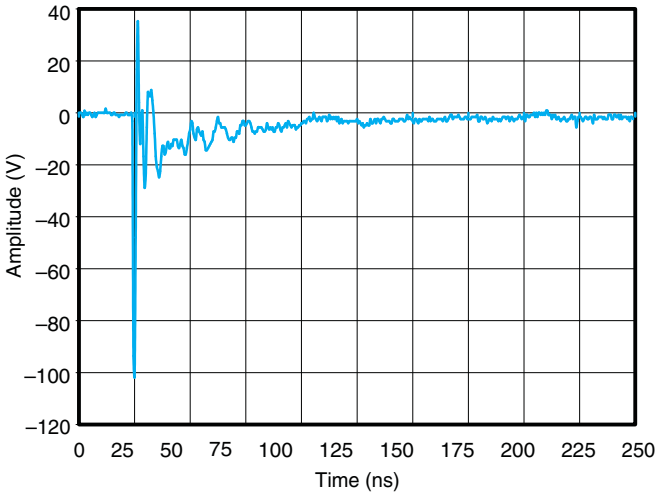

Figure 13. IEC Clamping Waveform, –8 kV Contact, D+, 25 ns/div

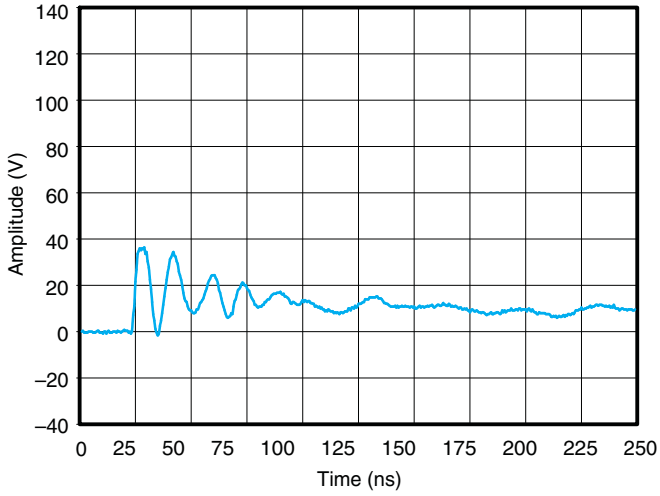

Figure 14. V_{BUS} IEC Clamping Waveform, 8 kV Contact, 25 ns/div

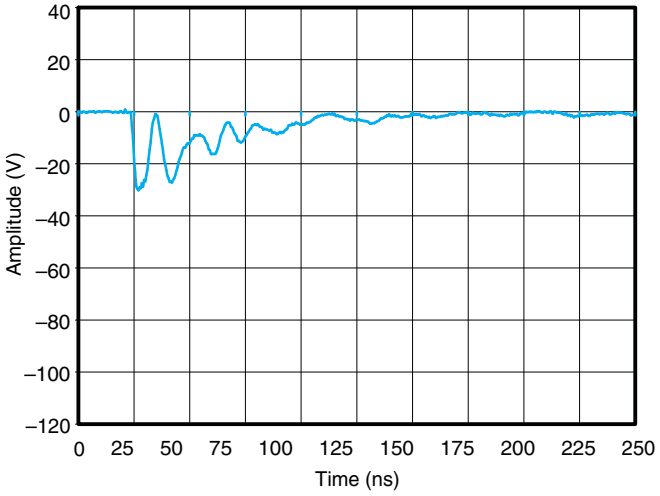

Figure 15. V_{BUS} IEC Clamping Waveform, –8 kV Contact, 25 ns/div

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9 Power Supply Recommendations

This family of devices are passive ESD protection devices and there is no need to power them. Care should be taken to not violate the maximum voltage specification to ensure that the device functions properly. The V_{BUS} TVS diode can tolerate up to a 15 V signal. The D+, D–, and ID pins tolerate up to a 5.5 V signal.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

This application is typical of a mobile USB platform with an ID pin in addition to the D+, D–, and V_{BUS} pins.

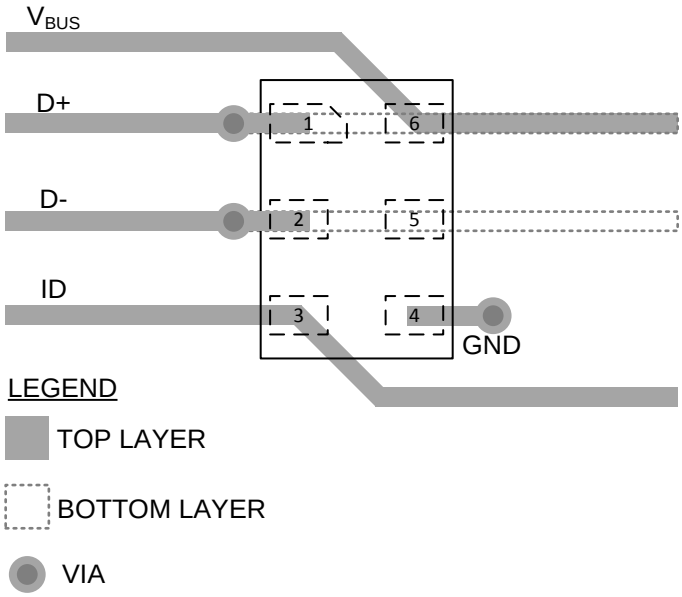

Figure 16. Using DRY Package

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11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4S012DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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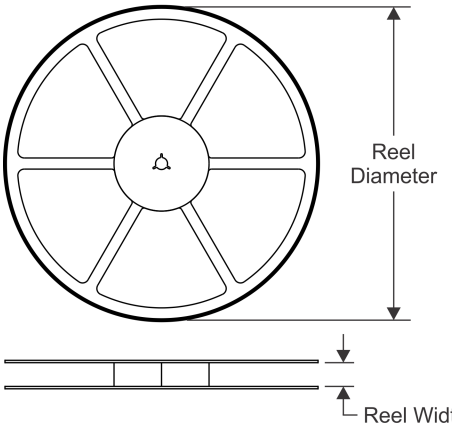
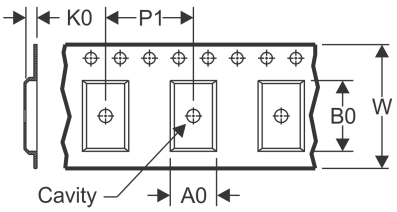
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

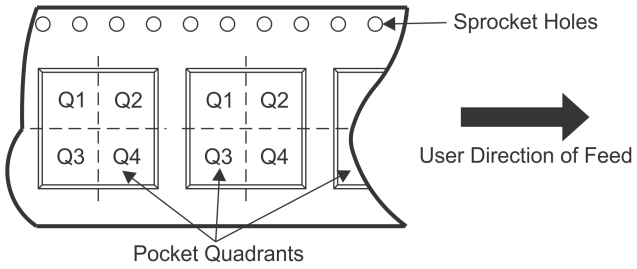


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

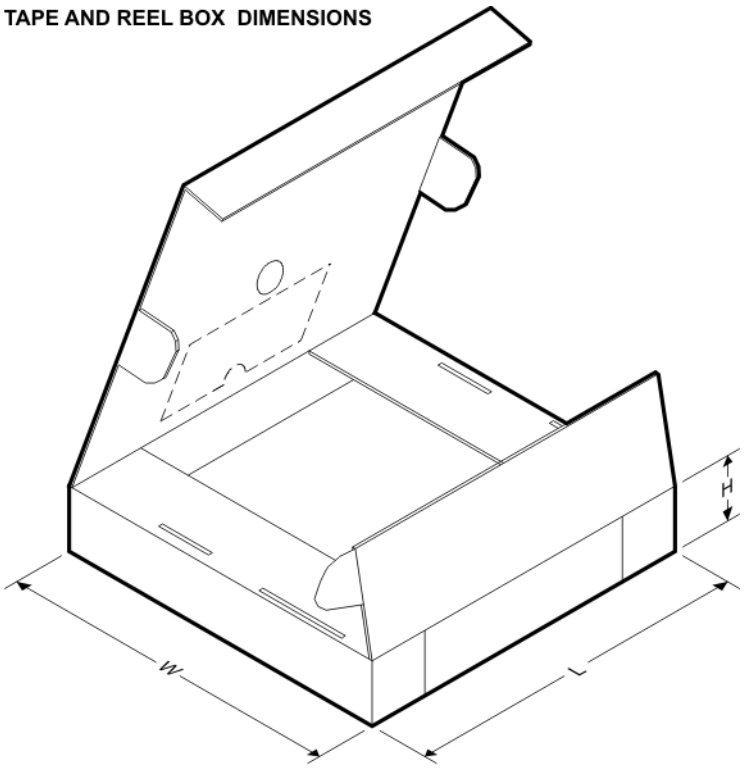
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S012DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

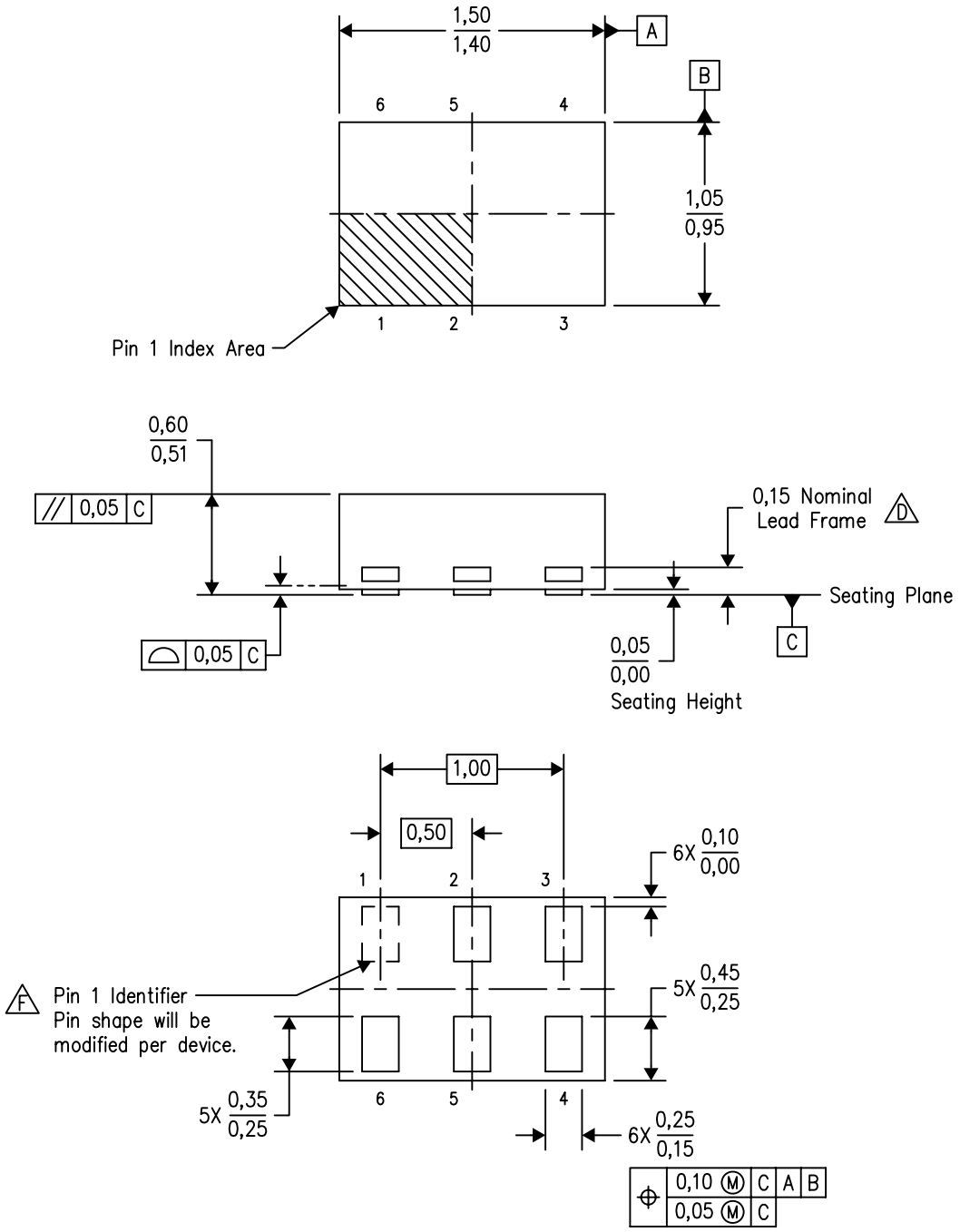
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S012DRYR	SON	DRY	6	5000	203.0	203.0	35.0

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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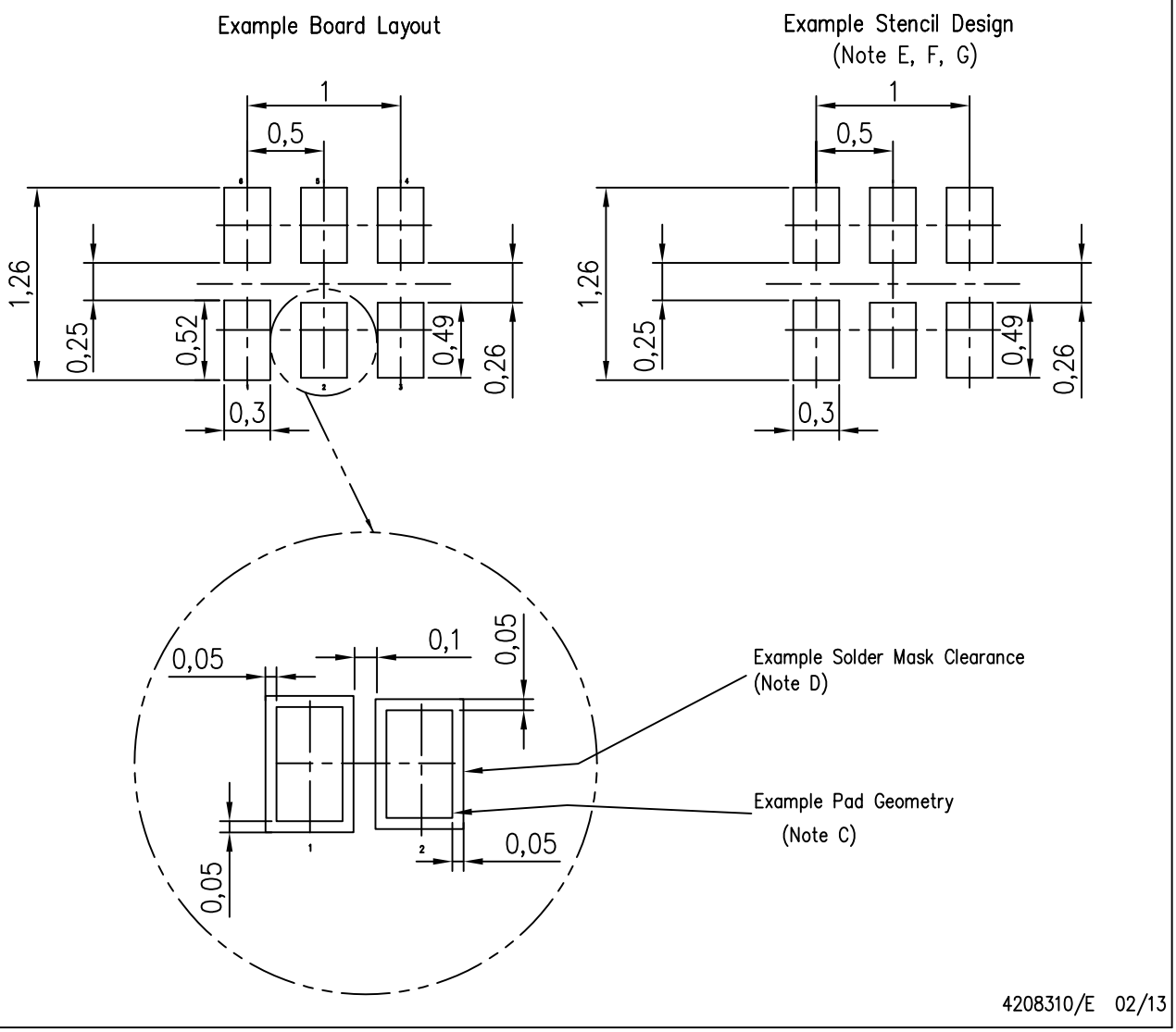
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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