LM2664 Switched Capacitor Voltage Converter

1 Features

- Inverts Input Supply Voltage
- 6-Pin SOT-23 Package
- 12-Ω Typical Output Impedance
- 91% Typical Conversion Efficiency at 40 mA
- 1-µA Typical Shutdown Current

2 Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

3 Description

The LM2664 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.8 V to 5.5 V to the corresponding negative voltage of −1.8 V to −5.5 V. The device uses two low-cost capacitors to provide up to 40 mA of output current.

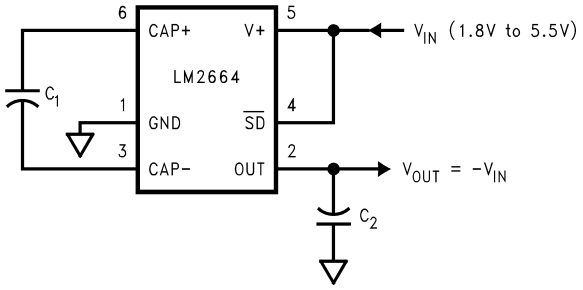
The LM2664 operates at 160-kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 220 µA (operating efficiency greater than 91% with most loads) and 1-µA typical shutdown current, the LM2664 provides ideal performance for battery-powered systems.

Device Information(1)

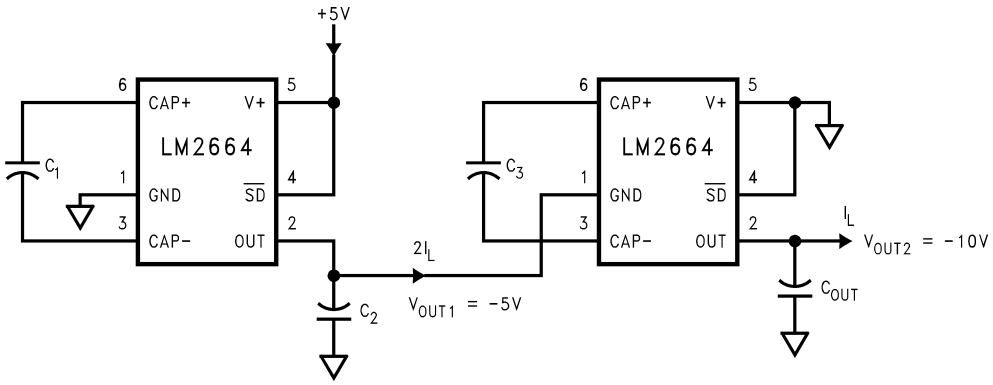
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2664	SOT-23 (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Voltage Inverter



5 V to −10 V Converter



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2013) to Revision E — **Page**

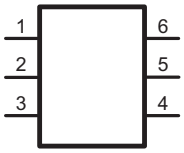
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (May 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 11

5 Pin Configuration and Functions

SOT-23 (DBV)
6 Pins
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	GND	Ground	Power supply ground input.
2	OUT	Power	Negative voltage output.
3	CAP−	Power	Connect this pin to the negative terminal of the charge-pump capacitor.
4	SD	Input	Shutdown control pin, tie this pin to V+ in normal operation, and to GND for shutdown.
5	V+	Power	Power supply positive voltage input.
6	CAP+	Power	Connect this pin to the positive terminal of the charge-pump capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or GND to OUT)		5.8	V
SD	(GND − 0.3)	(V+ + 0.3)	V
V+ and OUT continuous output current		50	mA
Output short-circuit duration to GND (3)		1	sec.
Continuous power dissipation (T_A = 25°C) (4)		600	mW
T_{JMax} (4)		150	°C
Lead temp. (soldering, 10 seconds)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)		2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating junction temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM2664 DBV 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

MIN and MAX limits apply over the full operating temperature range. Unless otherwise specified: T_J = 25°C, V+ = 5 V, C_1 = C_2 = 3.3 µF.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
V+	Supply voltage		1.8		5.5	V
I_Q	Supply current	No load		220	500	µA
I_{SD}	Shutdown supply current			1		µA
V_{SD}	Shutdown pin input voltage	Normal operation	2(4)			V
		Shutdown mode			0.8(5)	
I_L	Output current		40			mA
R_{SW}	Sum of the $R_{ds(on)}$ of the four internal MOSFET switches	I_L = 40 mA		4	8	Ω
R_{OUT}	Output resistance(6)	I_L = 40 mA		12	25	Ω
f_{OSC}	Oscillator frequency	See(7)	80	160		kHz
f_{SW}	Switching frequency	See(7)	40	80		kHz
P_{EFF}	Power efficiency	R_L (1 k) between GND and OUT	90%	94%		
		I_L = 40 mA to GND		91%		
V_{OEFF}	Voltage conversion efficiency	No load	99%	99.96%		

(1) In the test circuit, capacitors C_1 and C_2 are 3.3-µF, 0.3-Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.
(2) Min. and Max. limits are ensured by design, test, or statistical analysis.
(3) Typical numbers are not ensured but represent the most likely norm.
(4) The minimum input high for the shutdown pin equals 40% of V+.
(5) The maximum input low for the shutdown pin equals 20% of V+.
(6) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in *Application and Implementation* for simple negative voltage converter.
(7) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

6.6 Typical Characteristics

(Circuit of Figure 9 V+ = 5 V unless otherwise specified)

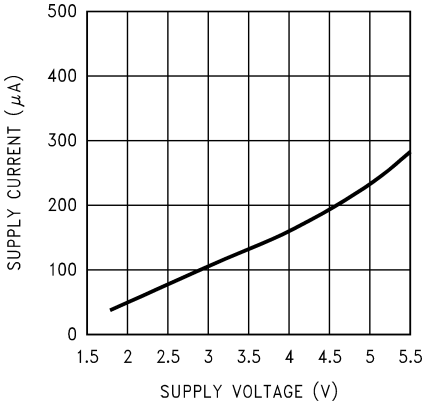


Figure 1. Supply Current vs Supply Voltage

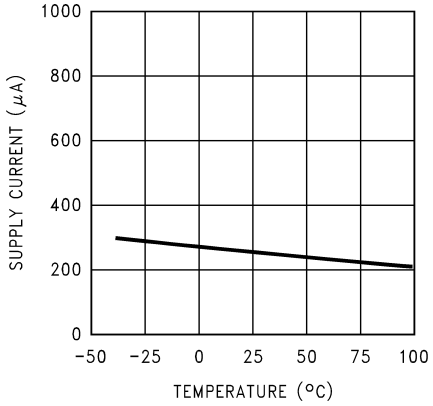


Figure 2. Supply Current vs Temperature

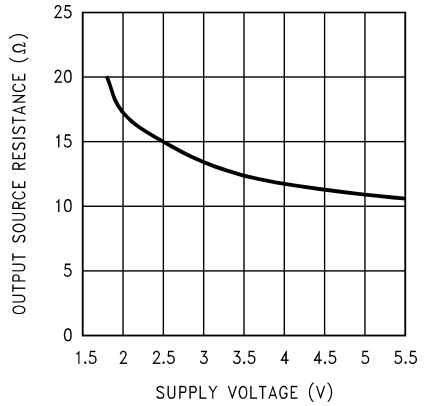


Figure 3. Output Source Resistance vs Supply Voltage

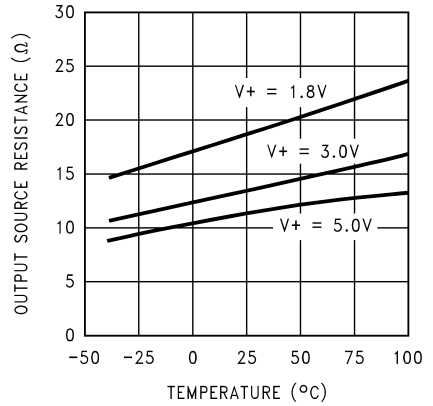


Figure 4. Output Source Resistance vs Temperature

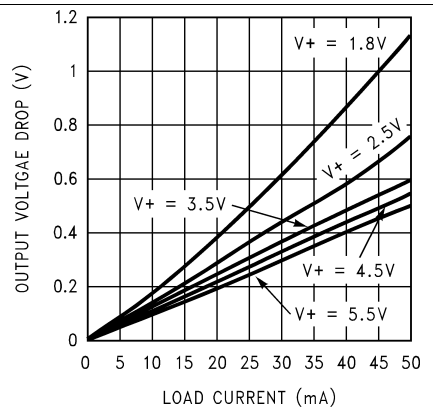


Figure 5. Output Voltage Drop vs Load Current

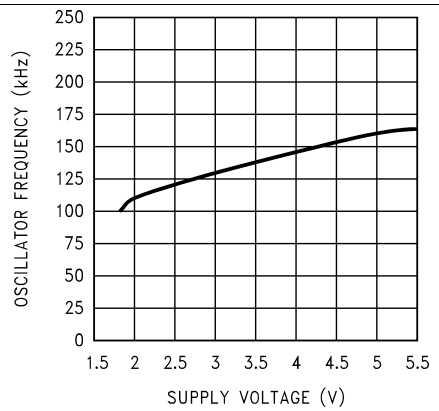


Figure 6. Oscillator Frequency vs Supply Voltage

Typical Characteristics (continued)

(Circuit of Figure 9 V+ = 5 V unless otherwise specified)

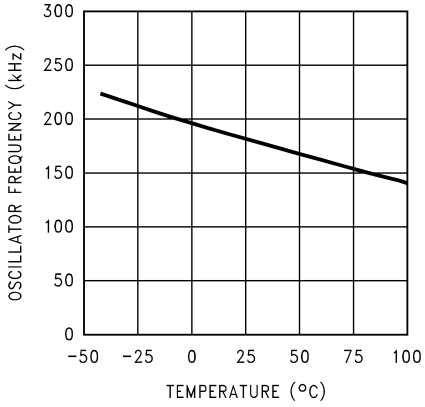


Figure 7. Oscillator Frequency vs Temperature

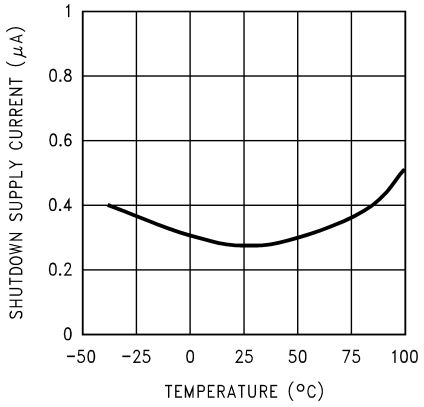
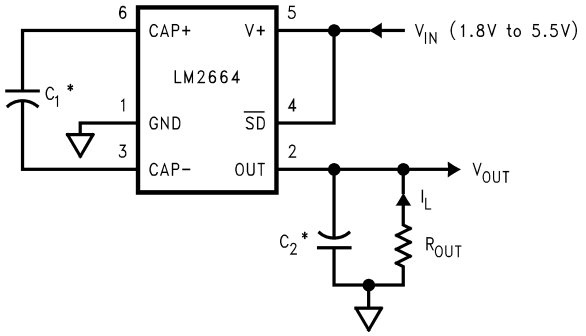


Figure 8. Shutdown Supply Current vs Temperature

7 Parameter Measurement Information

7.1 Test Circuit



*C_1 and C_2 are 3.3 µF, SC series OS-CON capacitors.

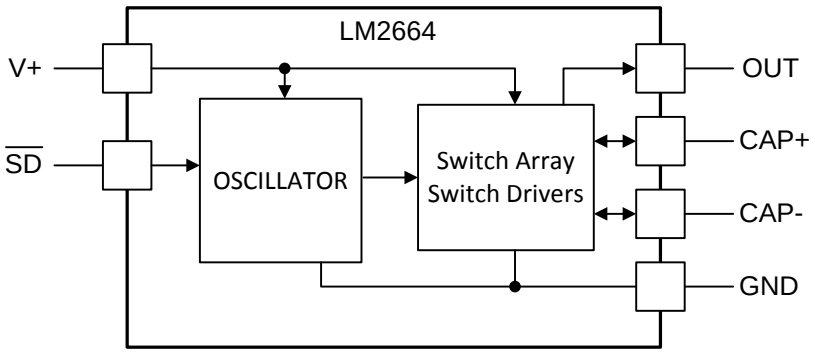
Figure 9. LM2664 Test Circuit

8 Detailed Description

8.1 Overview

The LM2664 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.8 V to 5.5 V to the corresponding negative voltage of −1.8 V to −5.5 V. The LM2664 uses two low-cost capacitors to provide up to 40 mA of output current.

8.2 Functional Block Diagram



8.3 Feature Description

The LM2664 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 10 illustrates the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V+. During this time interval, switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open; at the same time, S_2 and S_4 are closed, C_1 is charging C_2. After a number of cycles, the voltage across C_2 will be pumped to V+. Since the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(V+) when there is no load current. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details will be discussed in the following application information section.

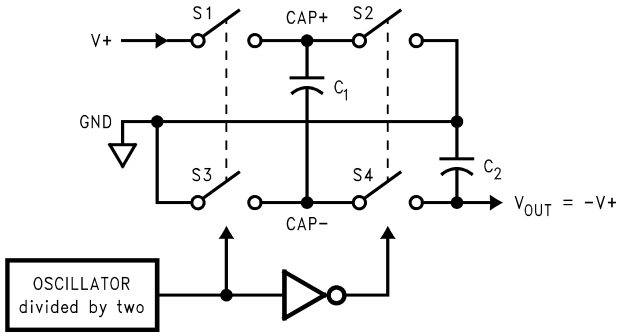


Figure 10. Voltage Inverting Principle

8.4 Device Functional Modes

8.4.1 Shutdown Mode

A shutdown ($\overline{SD}$) pin is available to disable the device and reduce the quiescent current to 1 µA. Applying a voltage less than 20% of V+ to the $\overline{SD}$ pin will bring the device into shutdown mode. While in normal operating mode, the pin is connected to V+.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM2664 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.8 V to 5.5 V to the corresponding negative voltage of −1.8 V to −5.5 V. The LM2664 uses two low cost capacitors to provide up to 40 mA of output current. The LM2664 operates at 160-kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 220 µA (operating efficiency greater than 91% with most loads) and 1 µA typical shutdown current, the LM2664 provides ideal performance for battery powered systems.

9.2 Typical Application - Voltage Inverter

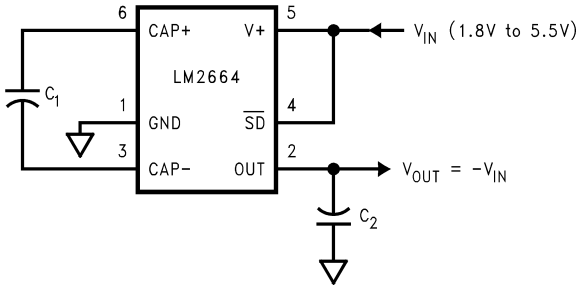


Figure 11. Voltage Inverter

9.2.1 Design Requirements

Example requirements for typical voltage inverter applications:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.8 V to 5.5 V
Output current	0 mA to 40 mA
Boost switching frequency	80 kHz

9.2.2 Detailed Design Requirements

The main application of LM2664 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in Voltage Inverter and 5 V to −10 V Converter. The range of the input supply voltage is 1.8 V to 5.5 V.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals −(V+). The output resistance R_{OUT} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance and equivalent series resistance (ESR) of C_1 and C_2. Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 will be multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of R_{OUT} is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 10.

High capacitance, low ESR capacitors will reduce the output resistance.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the output capacitor C_2:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

Again, using a low ESR capacitor will result in lower ripple.

9.2.2.1 Paralleling Devices

Any number of LM2664s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{OUT} is needed as shown in Figure 12. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT} \text{ of each LM2664}}{\text{Number of Devices}} \quad (3)$$

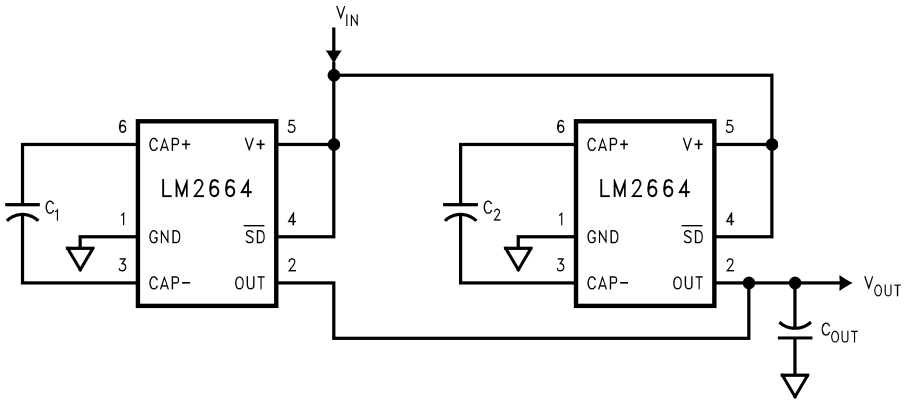


Figure 12. Lowering Output Resistance by Paralleling Devices

9.2.2.2 Cascading Devices

Cascading the LM2664 devices is an easy way to produce a greater negative voltage (a two-stage cascade circuit is shown in Figure 13).

If n is the integer representing the number of devices cascaded, the unloaded output voltage V_{out} is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{OUT} = nR_{out\_1} + n/2\ R_{OUT\_2} + ... + R_{OUT\_n} \quad (4)$$

NOTE

The number of n is practically limited since the increasing of n significantly reduces the efficiency, and increases the output resistance and output voltage ripple.

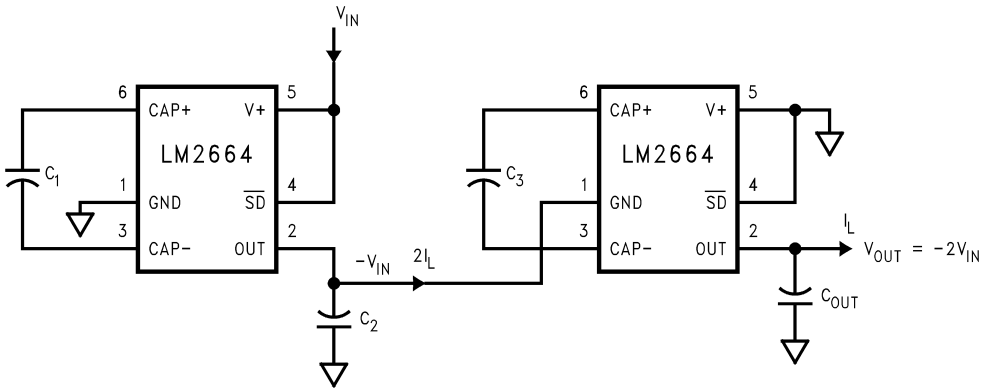


Figure 13. Increasing Output Voltage by Cascading Devices

9.2.2.3 Combined Doubler and Inverter

In Figure 14, the LM2664 is used to provide a positive voltage doubler and a negative voltage converter. Note that the total current drawn from the two outputs should not exceed 50 mA.

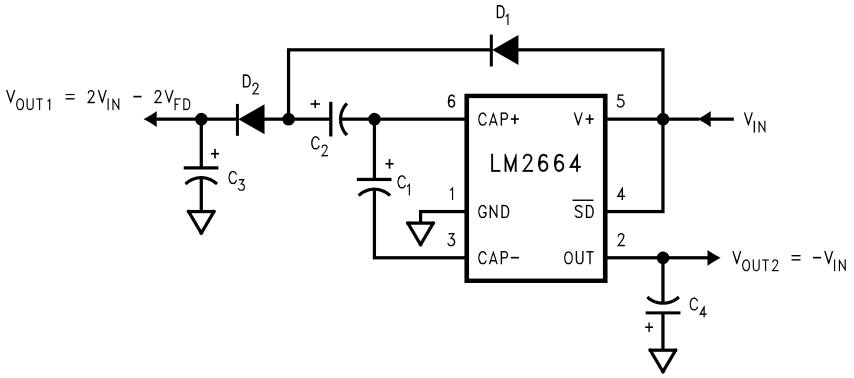


Figure 14. Combined Voltage Doubler and Inverter

9.2.2.4 Regulating V_{OUT}

It is possible to regulate the negative output of the LM2664 by use of a low dropout regulator (such as LP2980). The whole converter is depicted in Figure 15. This converter can give a regulated output from −1.8 V to −5.5 V by choosing the proper resistor ratio:

$$V_{OUT} = V_{ref} (1 + R_1/R_2) \quad (5)$$

where, $V_{ref} = 1.23$ V (6)

Note that the following conditions must be satisfied simultaneously for worst case design:

$$V_{in\_min} > V_{out\_min} + V_{drop\_max} \text{ (LP2980)} \quad (7)$$

$$+ I_{out\_max} \times R_{out\_max} \text{ (LM2664)} \quad (8)$$

$$V_{in\_max} < V_{out\_max} + V_{drop\_min} \text{ (LP2980)} \quad (9)$$

$$+ I_{out\_min} \times R_{out\_min} \text{ (LM2664)} \quad (10)$$

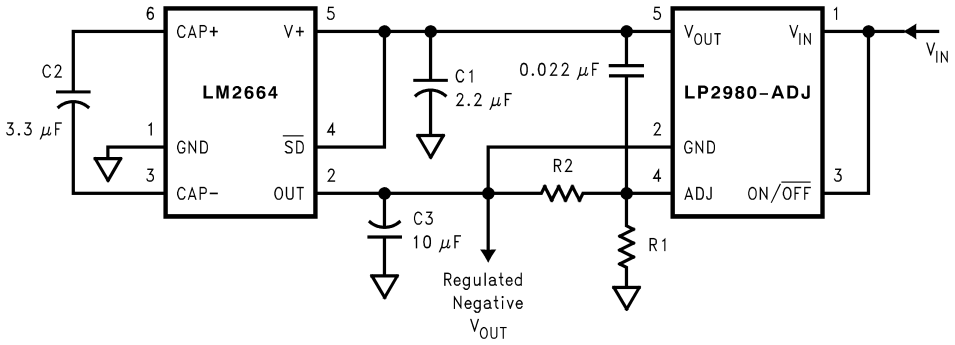


Figure 15. Combining LM2664 with LP2980 to Make a Negative Adjustable Regulator

9.2.2.5 Output Capacitor Selection

As discussed in *Detailed Design Requirements*, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{OUT} + I_Q (V+)} \tag{11}$$

Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $I_L^2 R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the specifications of the dropout voltage (which equals I_{out} R_{OUT}), the output voltage ripple, and the converter efficiency. Table 1 lists recommendations to maximize efficiency, reduce the output voltage drop and voltage ripple.

Table 1. Low ESR Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE
Nichicon Corp.	PL & PF series, through-hole aluminum electrolytic
AVX Corp.	TPS series, surface-mount tantalum
Sprague	593D, 594D, 595D series, surface-mount tantalum
Sanyo	OS-CON series, through-hole aluminum electrolytic
Murata	Ceramic chip capacitors
Taiyo Yuden	Ceramic chip capacitors
Tokin	Ceramic chip capacitors

9.2.3 Application Curve

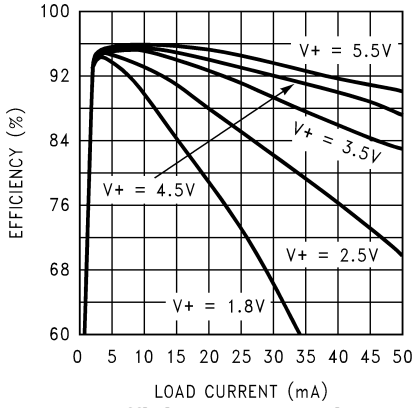


Figure 16. Efficiency vs Load Current

10 Power Supply Recommendations

The LM2664 is designed to operate from as an inverter over an input voltage supply range between 1.8 V and 5.5 V when the LV pin is grounded. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2664 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2664 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range

- Place C_{IN} on the top layer (same layer as the LM2664) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line
- Place C_{OUT} on the top layer (same layer as the LM2664) and as close as possible to the OUT and GND pin. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2664) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

11.2 Layout Example

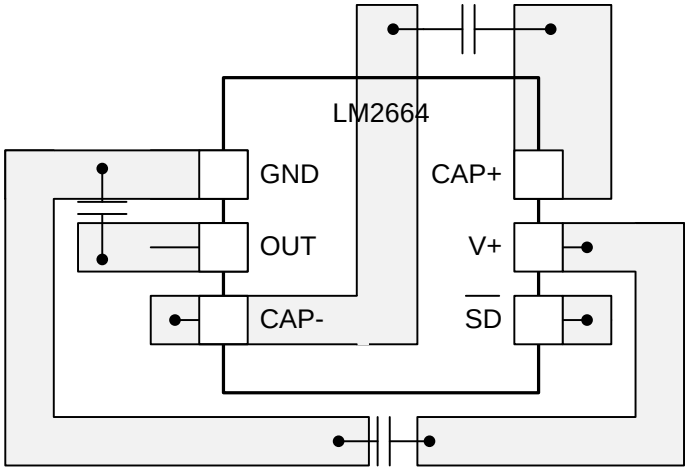


Figure 17. LM2664 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2664M6	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 85	S03A	
LM2664M6/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S03A	Samples
LM2664M6X	NRND	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 85	S03A	
LM2664M6X/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S03A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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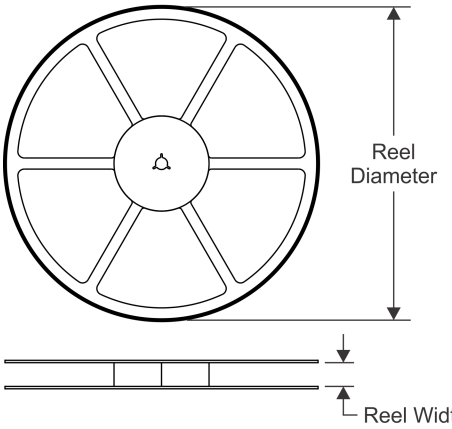
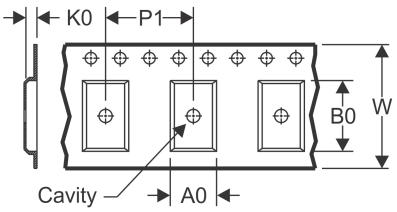
TAPE AND REEL INFORMATION

REEL DIMENSIONS

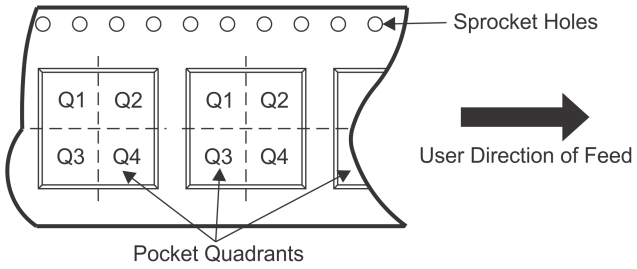


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

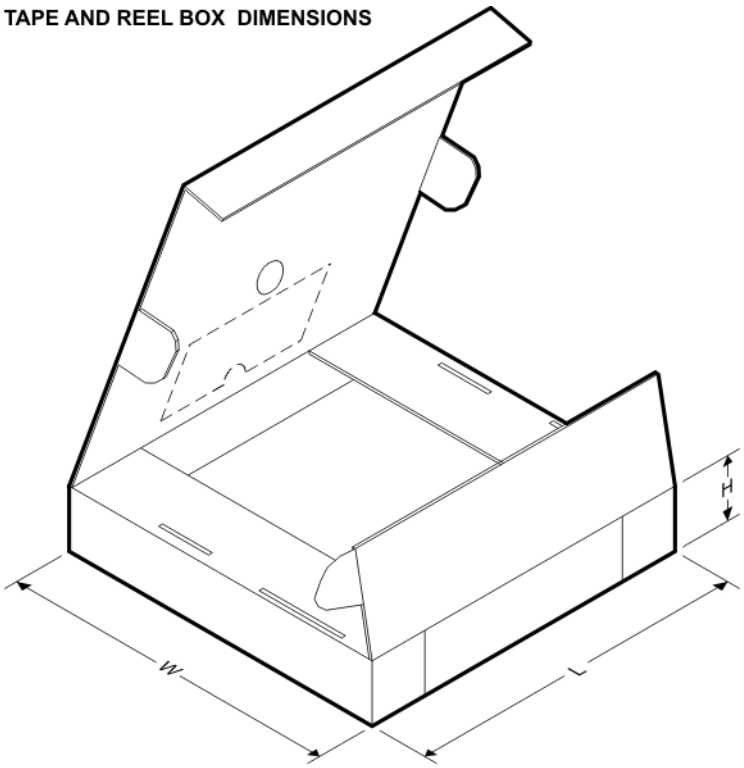
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2664M6	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2664M6/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2664M6X	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2664M6X/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

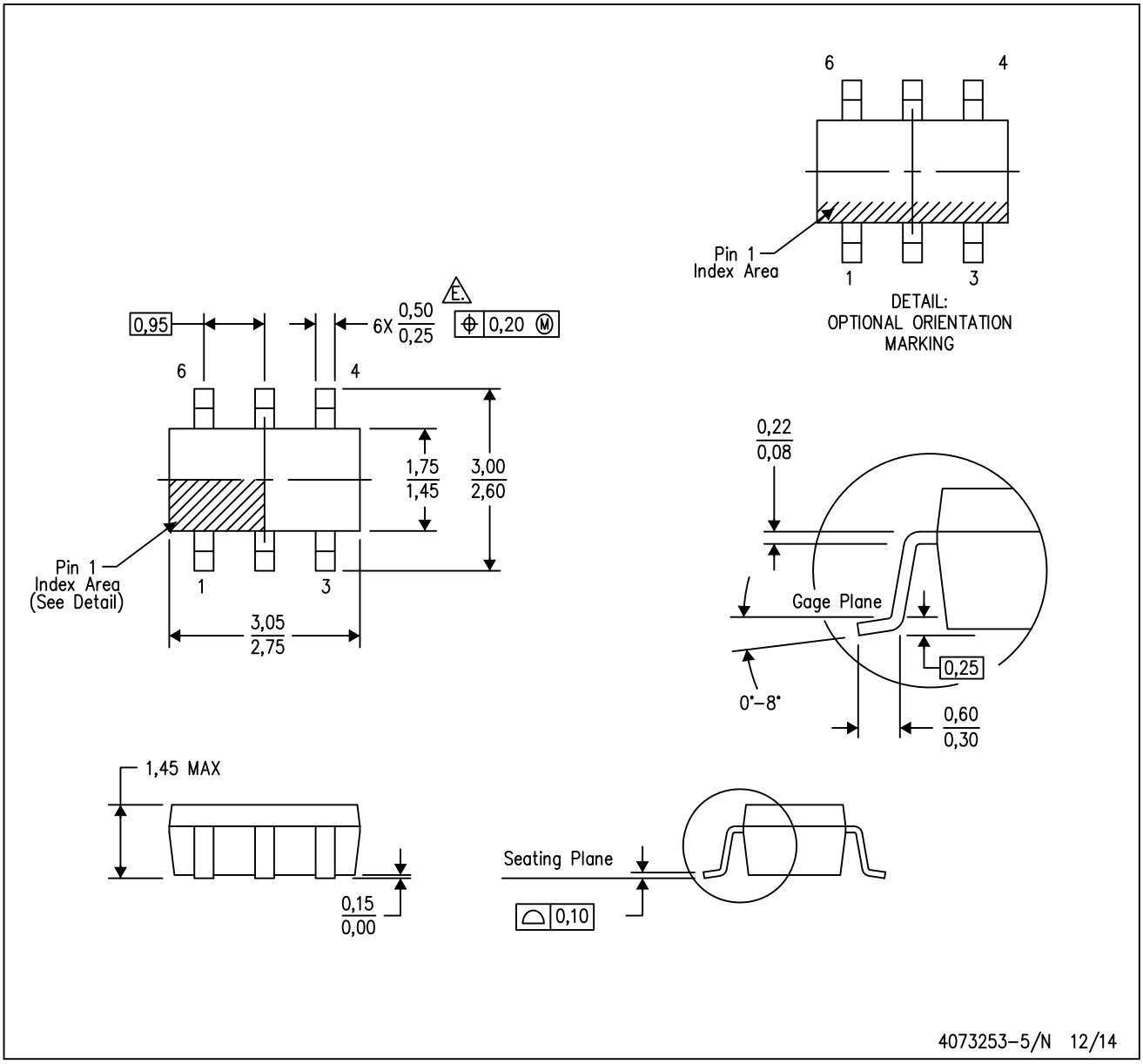
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2664M6	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM2664M6/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM2664M6X	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM2664M6X/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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