

DESCRIPTION

The IRF7828TRPBF is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance.

This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications

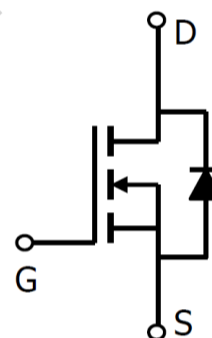
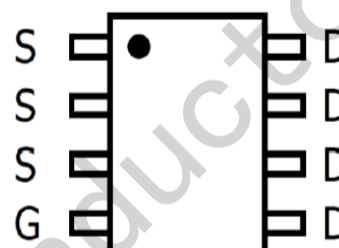
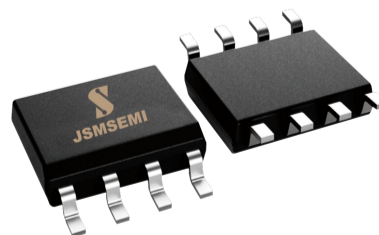
FEATURE

- ◆ 30V/15A, $R_{DS(ON)} = 8.5m\Omega$ (typ.)@ $V_{GS}=10V$
- ◆ 30V/11A, $R_{DS(ON)} = 14m\Omega$ (typ.)@ $V_{GS}=4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 package design

APPLICATIONS

- ◆ High Frequency Point-of-Load Synchronous
- ◆ Newworking DC-DC Power System
- ◆ Load Switch

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current ($T_A=25^\circ C$)	$V_{GS}=10V$	15	A
	Continuous Drain Current ($T_A=70^\circ C$)		12	a
I_{DM}	Pulsed Drain Current		40	A
I_S	Continuous Source Current (Diode Conduction)		2.0	A
P_D	Power Dissipation	$T_A=25^\circ C$	3.0	W
		$T_A=70^\circ C$	2.1	
T_J	Operation Junction Temperature		150	$^\circ C$
T_{STG}	Storage Temperature Range		-55~+150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		85	$^\circ C/W$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.9	3.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0$			1	uA
		$V_{DS}=24V, V_{GS}=0$ $T_J=55^\circ\text{C}$			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=15A$		8.5	11	m Ω
		$V_{GS}=4.5V, I_D=11A$		14	18	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=1.0A, V_{GS}=0V$		0.71	1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=15V$ $V_{GS}=4.5V$ $I_D=14A$		16	20.8	nC
Q_{gs}	Gate-Source Charge			5	6.5	
Q_{gd}	Gate-Drain Charge			3	3.9	
C_{iss}	Input Capacitance	$V_{DS}=15V$ $V_{GS}=0V$ $f=1\text{MHz}$		2470		pF
C_{oss}	Output Capacitance			325		
C_{rss}	Reverse Transfer Capacitance			185		
$T_{d(on)}$	Turn-On Time	$V_{DS}=15V$ $I_D=14A$		17	34	nS
T_r				5	10	
$T_{d(off)}$	Turn-Off Time	$V_{GEN}=10V$ $R_G=6\Omega$		50	100	
T_f				10	20	

Note: 1. Pulse test: pulse width \leq 300uS, duty cycle \leq 2%

2. Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS** (25°C Unless Note)

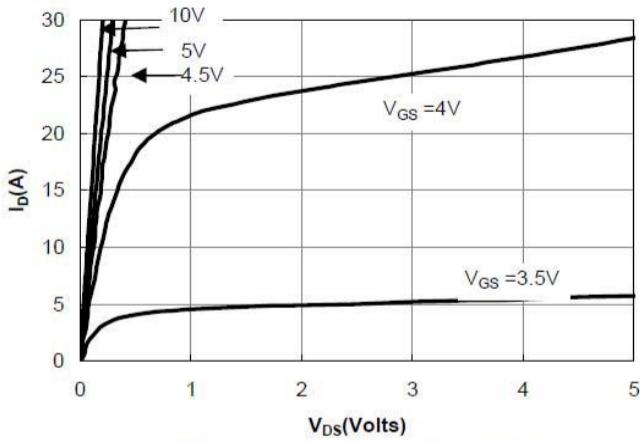


Figure 1: On-Regions Characteristics

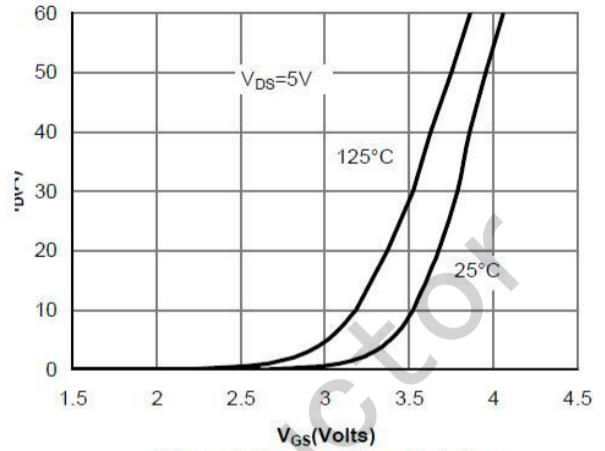


Figure 2: Transfer Characteristics

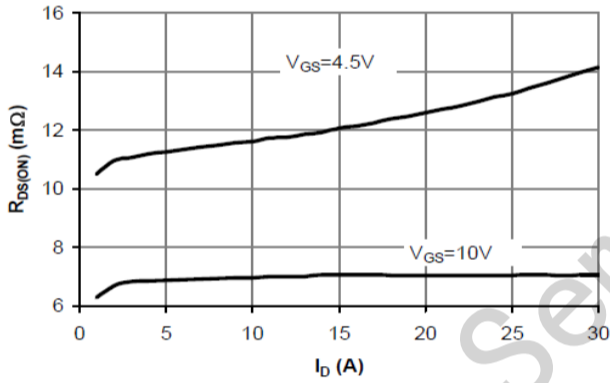


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

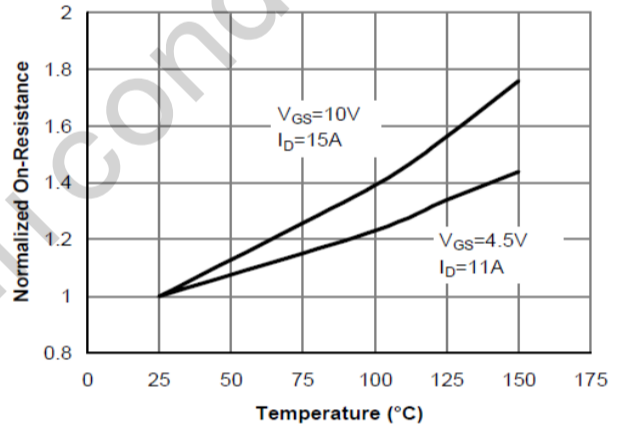


Figure 4: On-Resistance vs. Junction Temperature

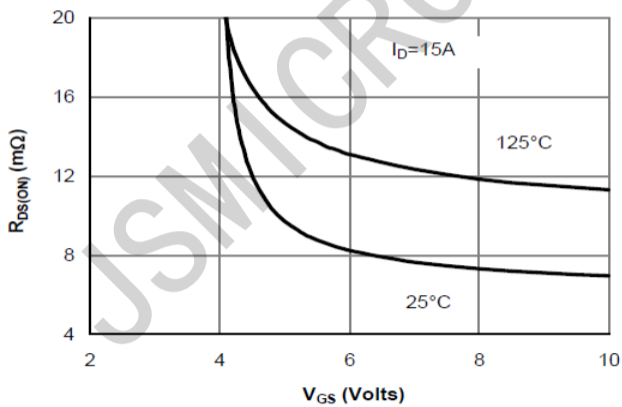


Figure 5: On-Resistance vs. Gate-Source Voltage

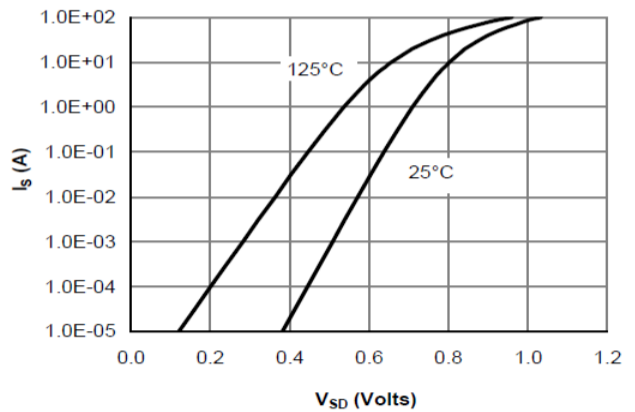


Figure 6: Body-Diode Characteristics

■ **TYPICAL CHARACTERISTICS** (continuous)

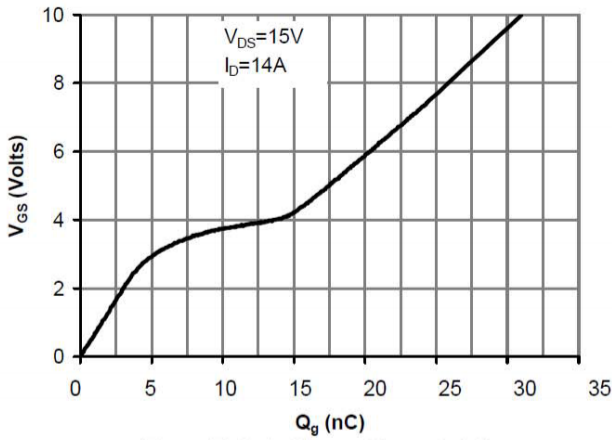


Figure 7: Gate-Charge Characteristics

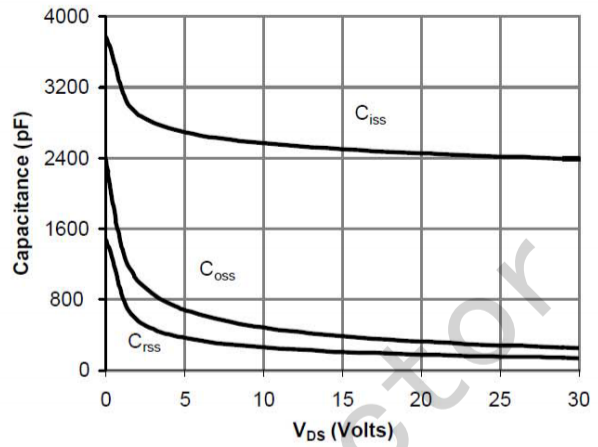


Figure 8: Capacitance Characteristics

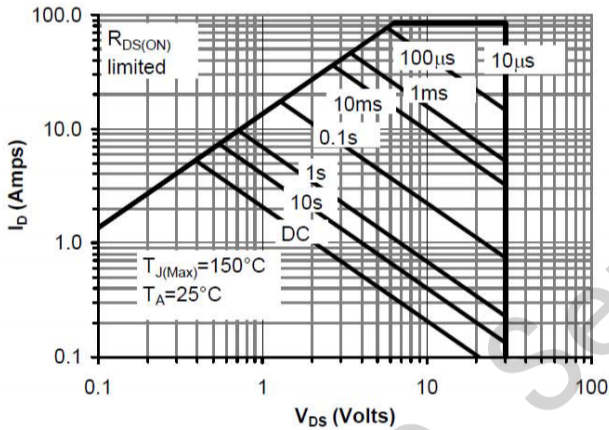


Figure 9: Maximum Forward Biased Safe Operating Area

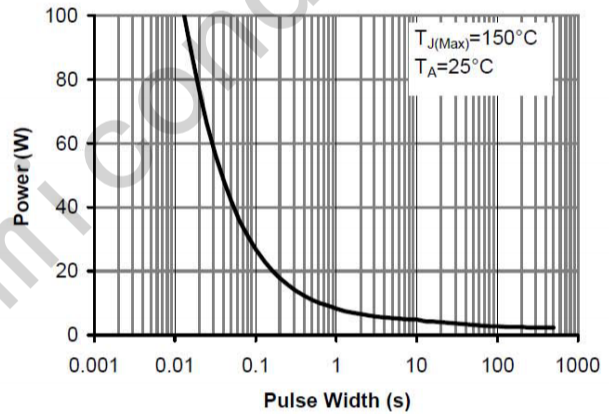


Figure 10: Single Pulse Power Rating Junction-to-Ambient

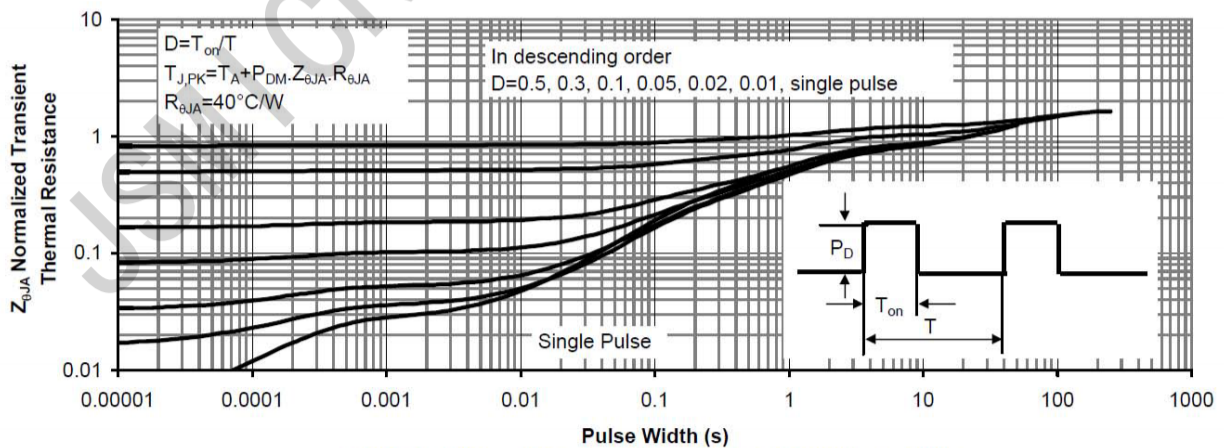
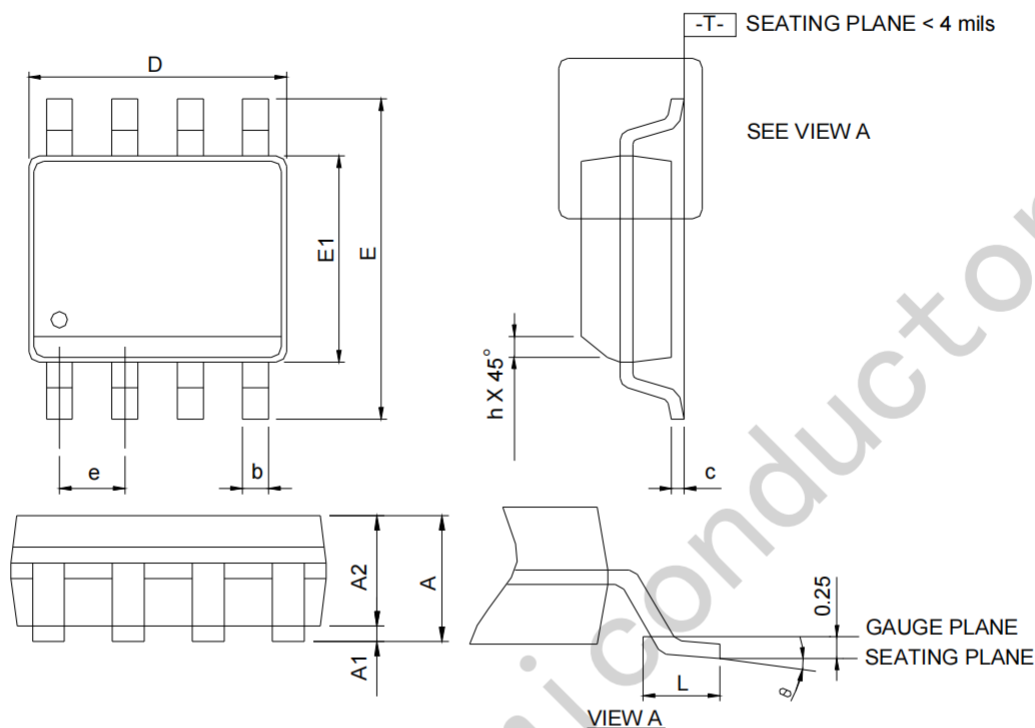


Figure 11: Normalized Maximum Transient Thermal Impedance

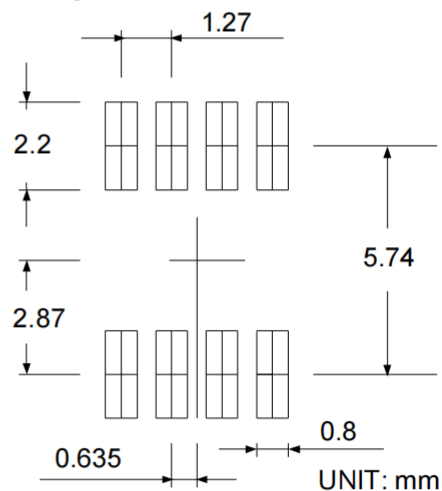
Package Information

SOP-8



SYMBOLS	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.